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| EXAMINER | |
|---|---|
| VITAL, PIERRE M | |

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| 2188 | 13 |

DATE MAILED: 05/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/651,488 | Applicant(s) ENGLIN ET AL. | |
|---|---|---|---|
| | Examiner Pierre M. Vital | Art Unit 2188 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6 and 11-20* is/are rejected.

7)☒ Claim(s) *4-5, 7-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

1. This Office Action is in response to applicant's communication filed February 19, 2004 in response to PTO Office Action mailed November 14, 2003. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. Claims 1-20 have been presented for examination in this application. In response to the last Office Action, claims 1, 2, 4, 6, 7, 10, 11 and 16-20 have been amended. No claims have been canceled or added. As a result, claims 1-20 are now pending in this application.

3. The objection to claim 2 has been withdrawn due to the amendment filed February 19, 2004.

4. The rejection of claims 1-20 as in the Office action mailed November 14, 2003 (Paper No. 11) has been withdrawn due to the amendment filed February 19, 2004. New grounds of rejection follow herewith.

### *Response to Arguments*

5. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grice et al (US5,426,754) and Matick et al (US6,081,872).

As per claim 1, Grice discloses in a data processing system having a processor responsively coupled to a store in cache memory which is responsively coupled to a lower level memory, the improvement comprising:

a. a read-only level-one instruction cache memory directly coupled to said processor [*CPU contains an instruction cache which is read only*; col. 8, lines 1-3];

b. a store-through level one operand cache memory directly coupled to said processor [*first level data caches are store through*; col. 7, lines 23-27];

c. wherein said processor is responsively coupled to said store-in cache memory via said read-only level one instruction cache memory and via said store-through level one operand cache memory [*CPU connected to L2 via L1*; col. 2, lines 12-19].

However, Grice does not specifically teach a flush buffer directly coupled to said store-in cache memory and said lower level memory as recited in the claim.

Matick discloses a store back buffer (i.e., flush buffer) coupled to a store-in L2 cache and an L3 cache to provide a multi-cycle transfer for a castout to L3 cache or main memory (*register 149*; Fig. 9; col. 8, lines 3-15). Since the technology for implementing a

flush buffer coupled to a store-in L2 and an L3 cache was well known and since a flush buffer coupled to a store-in L2 cache and an L3 cache provides a multi-cycle transfer for a castout to L3 cache or main memory, an artisan would have been motivated to implement a flush buffer coupled to a store-in L2 and an L3 cache in the system of Grice. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a flush buffer coupled to a store-in L2 cache and an L3 cache because it was well known to provide a multi-cycle transfer for a castout to L3 cache or main memory as taught by Matick.

As per claim 6, Grice discloses a data processing system comprising:

a. A processor [*processor 100*; Fig. 1];

b. A level one store-through cache memory having a read-only instruction portion and an operand portion directly coupled to said processor [*CPU contains an instruction cache which is read only*; col. 8, lines 1-3; *first level data caches are store through*; col. 7, lines 23-27];

c. A store-in cache memory responsively coupled to said processor via said read-only instruction portion and said operand portion of said level one store-through cache memory [*CPU connected to L2 via L1*; col. 2, lines 12-19].

d. A lower level memory responsively coupled to said store-in cache memory [*main storage 101 coupled to L2 cache*; Fig. 1].

However, Grice does not specifically teach a flush buffer directly coupled to said store-in cache memory and said lower level memory as recited in the claim.

Matick discloses a store back buffer (i.e., flush buffer) coupled to a store-in L2 cache and an L3 cache to provide a multi-cycle transfer for a castout to L3 cache or main memory (*register 149*; Fig. 9; col. 8, lines 3-15). Since the technology for implementing a flush buffer coupled to a store-in L2 and an L3 cache was well known and since a flush buffer coupled to a store-in L2 cache and an L3 cache provides a multi-cycle transfer for a castout to L3 cache or main memory, an artisan would have been motivated to implement a flush buffer coupled to a store-in L2 and an L3 cache in the system of Grice. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a flush buffer coupled to a store-in L2 cache and an L3 cache because it was well known to provide a multi-cycle transfer for a castout to L3 cache or main memory as taught by Matick.

8. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grice et al (US5,426,754) and Matick et al (US6,081,872) and further in view of Freerksen et al (US6,314,491).

As per claim 2, Grice and Matick disclose the claimed invention as detailed above in the previous paragraphs. However Grice and Matick do not specifically teach a tag memory responsively coupled to said store-in cache memory which indicates whether a particular location within said store-in memory has been modified by said processor as recited in the claim.

Freerksen discloses a tag field coupled to a L2 cache to manage replacement of lines by identifying the address in main storage to which the data in cache corresponds (col. 7, lines 15-31). Since the technology for implementing a tag memory coupled to a cache was well known and since a tag memory coupled to a store-in cache mages replacement of lines by identifying the address in main storage to which the data in cache corresponds, an artisan would have been motivated to implement a tag memory coupled to a store-in cache in the system of Grice and Matick. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a tag memory coupled to a store-in cache because it was well known to manage replacement of lines by identifying the address in main storage to which the data in cache corresponds as taught by Freerksen.

As per claim 3, Freerksen discloses a logic circuit which loads said flush buffer with data from said particular location within said store-in cache memory in response to said indication that said particular location within said store-in memory has been modified by the processor [*logic in storage control unit 22 manages the process of obtaining and delivering to/from cache buffer 30*; col. 7, lines 1-13; *a flush write back command is generated when there is a modified version in the line in the L1 cache*; col. 8, line 61 – col. 9, line 11].

9. Claims 11-12, and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Freerksen et al (US6,314,491) and Grice et al (US5,426,754).

As per claim 11, Freerksen discloses a method of flushing a store-in cache memory responsively coupled to a level one store-through operand cache memory comprising:

a. receiving a data request at said store-in cache memory from said level one store-through operand cache memory [*processor 24 interacts with L1 cache to obtain and store needed data*; col. 5, lines 26-28; *L1 cache is a write back cache (also known as a store-in cache in the art)*; col. 6, line 64 – col. 7, line 4];

b. searching said store-in cache memory in response to said data request [*directory identifies memory location for which copies currently reside in*; col. 5, lines 41-46];

c. experiencing a cache miss in response to said searching step [*L1 cache is not storing the requested data*; col. 5, lines 53-59];

e. selecting a particular location within said store-in cache memory to be flushed buffer [*when there is a miss in L1 cache, a line in cache buffer 30 is assigned to the miss*; col. 6, lines 58 – col. 7, line 4]; transferring data from said particular location to a flush buffer [*when there is a miss in L1 cache, a line in cache buffer 30 is assigned to the miss, the data is stored in the assigned line of cache buffer 30*; col. 6, lines 58-64].

However, Freerksen does not specifically teach a store-in cache memory responsively coupled to a level one store-through operand cache memory as recited in the claim.

Grice discloses a store-in L2 cache memory to reduce the store bus traffic to main memory (col. 2, lines 12-14) responsively coupled to a level one store-through operand cache memory to maintain a logically coherent system memory (col. 7, lines 24-27). Since the technology for implementing a store-in L2 cache memory and a level one store-through operand cache memory was well known and since a store-in L2 cache memory reduces the store bus traffic to main memory and a level one store-through operand cache memory maintains a logically coherent system memory, an artisan would have been motivated to implement a store-in cache memory responsively coupled to a level one store-through operand cache memory in the system of Freerksen. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a store-in cache memory responsively coupled to a level one store-through operand cache memory because a store-in L2 cache memory reduces the store bus traffic to main memory and a level one store-through operand cache memory maintains a logically coherent system memory as taught by Grice.

As per claim 12, Freerksen discloses determining whether a particular location was modified by a processor [*the located cache line (CL) is evaluated to determine whether it is marked "modified"*; col. 7, lines 64 – col. 8, line 4].

As per claim 16, Freerksen discloses an apparatus comprising:

a. executing means for executing program instructions [*processors 24a, 24b*; Fig.2; col. 1, lines 12-15];

handling means responsively coupled to said executing means for handling operands in a level one cache memory [*control unit 22 coupled to processors 24*; Fig. 2];

b. caching means responsively coupled to said handling means for caching data [*L2 cache 26 couple to control unit 22*; Fig.2];

c. buffering means directly coupled to said caching means for buffering data from said caching means to be flushed [*intermediate cache buffer 30 is directly coupled to L2 caches 22*; Fig. 2; *data is cast back into cache buffer 30 which is an intermediate storage area*; col. 6, lines 41 – col. 7, line 4].

However, Freerksen does not specifically teach a store-through level one cache memory and caching data on a store-in basis as recited in the claim.

Grice discloses a store-in L2 cache memory to reduce the store bus traffic to main memory (col. 2, lines 12-14) responsively coupled to a level one store-through operand cache memory to maintain a logically coherent system memory (col. 7, lines 24-27). Since the technology for implementing a store-in L2 cache memory and a level one store-through operand cache memory was well known and since a store-in L2 cache memory reduces the store bus traffic to main memory and a level one store-through operand cache memory maintains a logically coherent system memory, an artisan would have been motivated to implement a store-in cache memory responsively coupled to a level one store-through operand cache memory in the system of

Freerksen. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a store-in cache memory responsively coupled to a level one store-through operand cache memory because a store-in L2 cache memory reduces the store bus traffic to main memory and a level one store-through operand cache memory maintains a logically coherent system memory as taught by Grice.

As per claim 17, Freerksen discloses means responsively coupled to said caching means for selecting said data to be flushed [*logic in storage control unit 22 manages the process of obtaining and delivering to/from cache buffer 30*; col. 7, lines 1-13].

10. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Freerksen et al (US6,314,491) and Grice et al (US5,426,754) and further in view of Jeddeloh (US6,460,114).

As per claim 13, Freerksen and Grice disclose the claimed invention as detailed above in the previous paragraphs. However, Freerksen and Grice do not specifically teach inhibiting said transferring step if said determining step determines that said data within said particular location was not modified by said processor as recited in the claim.

Jeddeloh discloses inhibiting a transferring step if a determining step determines that the data within a particular location was not modified by a processor (*clean data not transferred to temporary buffer*; col. 2, lines 5-10) to reduce the memory latency time

experienced by the CPU by selecting an existing cache line for replacement based on a status indication (col. 2, lines 1-24). Since the technology for inhibiting a transferring step when it is determined that data within a particular location was not modified by a processor was well known in the state of the art, and since inhibiting a transferring step when it is determined that data within a particular location was not modified by a processor reduces the memory latency time experienced by the CPU by selecting an existing cache line for replacement based on a status indication, an artisan in the art would have been motivated to implement inhibiting a transferring step when it is determined that data within a particular location was not modified by a processor in the system of Freerksen and Grice. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement inhibiting a transferring step when it is determined that data within a particular location was not modified because it was well known to reduce the memory latency time experienced by the CPU by selecting an existing cache line for replacement based on a status indication as taught by Jeddeloh.

11. Claims 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Freerksen et al (US6,314,491) and Grice et al (US5,426,754) and Jeddeloh (US6,460,114) and Kurosawa (US6,418,515).

As per claim 14, the combination of Freerksen and Grice and Jeddeloh discloses the claimed invention as detailed above in the previous paragraphs. However, the

combination of Freerksen and Grice and Jeddeloh does not specifically teach routing said data from said particular location to an available one of said first flush store and said second buffer store as recited in the claim.

Kurosawa discloses routing data from a particular location to an available one of a first flush buffer store and a second buffer store [*data is registered in the write-back buffer 403 at the second stage when write-back buffer 402 becomes free*; col. 29, lines 11-58; Fig. 2].

It would have been obvious to one of ordinary skill in the art, having the teachings of Freerksen and Grice and Jeddeloh and Kurosawa before him at the time the invention was made, to modify the system of Freerksen and Grice and Jeddeloh to include routing data from a particular location to an available one of a first flush buffer store and said second buffer store because it was well known to provide a cache flush unit which implement a quick cache flush and reduce overhead in checkpoint processing by allowing the cache information updating by the cache flush operation that can be executed in parallel [col. 26, lines 45-58] as taught by Kurosawa.

As per claim 15, Freerksen discloses rewriting said data to a lower level memory following said transferring step [*data in cache buffer is transferred to L2 cache or main memory*; col. 7, lines 1-4].

12. Claims 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Freerksen et al (US6,314,491) and Grice et al (US5,426,754) and Kurosawa (US6,418,515).

As per claim 18, Freerksen and Grice disclose the claimed invention as detailed above in the previous paragraphs. However, Freerksen and Grice do not specifically teach a flush buffer comprises a first flush buffer store having a first input and a first output and a second flush buffer store having a second input and a second output as recited in the claims.

Kurosawa discloses a flush buffer comprises a first flush buffer store having a first input and a first output and a second flush buffer store having a second input and a second output [*cache flush unit comprises write-back buffer 401 and write-back buffer 403 for cache flush*; col. 26, lines 31-40; *each write-back buffer has an input and an output*; Fig. 2].

It would have been obvious to one of ordinary skill in the art, having the teachings of Freerksen and Grice and Kurosawa before him at the time the invention was made, to modify the system of Freerksen and Grice to include a flush buffer comprises a first flush buffer store having a first input and a first output and a second flush buffer store having a second input and a second output because it was well known to provide a cache flush unit which implement a quick cache flush and reduce overhead in checkpoint processing by allowing the cache information updating by the cache flush operation that can be executed in parallel [col. 26, lines 45-58] as taught by Kurosawa.

As per claim 19, Freerksen and Grice disclose the claimed invention as detailed above in the previous paragraphs. However, Freerksen and Grice do not specifically teach a temporary register coupled to a store-in cache memory, a first flush buffer store and a second flush buffer store which routes said data from said particular location to an available one of said first flush store and said second buffer store as recited in the claims.

Kurosawa discloses a temporary register coupled to a store-in cache memory, a first flush buffer store and a second flush buffer store which routes said data from said particular location to an available one of said first flush store and said second buffer [*prefetching buffer 322 coupled to write-back buffers 401-403, data is registered in the write-back buffer 403 at the second stage when write-back buffer 402 becomes free*; col. 29, lines 11-58; Fig. 2].

It would have been obvious to one of ordinary skill in the art, having the teachings of Freerksen and Grice and Kurosawa before him at the time the invention was made, to modify the system of Freerksen and Grice to include a temporary register coupled to a store-in cache memory, a first flush buffer store and a second flush buffer store which routes said data from said particular location to an available one of said first flush store and said second buffer because it was well known to shorten the searching time associated with cache flush by checking the value of a bit to determine whether the data is received by the prefetching buffer [col. 30, lines 8-10] and provide a cache flush unit which implement a quick cache flush and reduce overhead in checkpoint processing by allowing the cache information updating by the cache flush operation that can be executed in parallel [col. 26, lines 45-58] as taught by Kurosawa.

13. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Freerksen et al (US6,314,491) and Grice et al (US5,426,754) and Kurosawa (US6,418,515) and Jeddeloh (US6,460,114).

As per claim 20, the combination of Freerksen and Grice and Kurosawa discloses the claimed invention as detailed above in the previous paragraphs.

Freerksen further discloses means responsively coupled to said caching means for determining whether data has been modified by said executing means [*cache line 52 comprises a tag field which identifies the address of the data and state field identifies the state of the line*; col. 7, lines 32-43].

However, the combination of Freerksen and Grice and Kurosawa does not specifically teach means responsively coupled to said determining means and said buffering means for inhibiting transfer of data from said caching means to said buffering means if said determining means determines that said data has not been modified by said executing means as recited in the claim.

Jeddeloh discloses means responsively coupled to a determining means and a buffering means for inhibiting transfer of data from a caching means to a buffering means if said determining means determines that said data has not been modified by an executing means [*clean data not transferred to temporary buffer*; col. 2, lines 5-10].

It would have been obvious to one of ordinary skill in the art, having the teachings of Freerksen and Grice and Kurosawa and Jeddeloh before him at the time the invention was made, to modify the system of Freerksen and Grice and Kurosawa to

include means responsively coupled to a determining means and a buffering means for inhibiting transfer of data from a caching means to a buffering means if said determining means determines that said data has not been modified by an executing means because it was well known to reduce the memory latency time experienced by the CPU by selecting an existing cache line for replacement based on a status indication [col. 2, lines 1-24] as taught by Jeddeloh.

***Allowable Subject Matter***

14. Claims 4-5 and 7-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. The following is a statement of reasons for the indication of allowable subject matter:

As per claims 4 and 7, the prior art of record does not teach or suggest "a flush buffer further comprising a first flush buffer store having a first input responsively coupled to a store-in cache memory and a first output directly coupled to a lower level memory and a second flush buffer store having a second input responsively coupled to said store-in cache memory and a second output directly coupled to said lower level memory in combination with the other elements set forth in the claimed invention. Therefore, dependent claims 5 and 8-10 are allowable as being dependent upon independent claims 4 and 7 and having additional allowable features therein.

***Conclusion***

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111 (c) to consider these references fully when responding to this action. The documents cited therein teach second level cache flushing, second level store-in cache, first level store-through cache, flush buffer coupled to store-in cache and cache line modification.

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April 29, 2004

Pierre M. Vital
Examiner
Art Unit 2188